

## Advance Information

This document contains information on a product under development.  
As such, it contains target parameters that are subject to change.

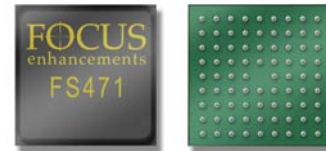


# FS471/472

## Video Encoder for battery operated handheld devices

### Features

- Designed for battery operated handheld devices
- Advanced power management enables sleep mode current of 20uA
- Load sensing video outputs
- Two 10 bit DACs supporting S-Video or CVBS video output
- Multiple output analog formats: NTSC, NTSC-EIAJ, PAL (B/G/H/I/M/N/60)
- Closed Captioning, CGMS-A, and WSS supported
- Macrovision 7.1L1 copy protection - FS472
- ITU-R BT.656/601 video input modes supported
- Programmable input interface (24 / 18 / 16 / 15 / 12 and 8 bit)
- Supports various RGB and YCrCb input formats, and resolutions from 220x176 to 1366x768
- Adjustable brightness, contrast and saturation
- Advanced 2D up / down scaler
- Advanced Flicker Filter
- Supports single or double termination
- Supports AC and DC coupled TV sets
- ITU-R BT.656 and VESA VIP digital output interface
- Master and Slave mode operations
- Flexible input clock frequency from the crystal or from the graphics controller (2.5MHz-85MHz)
- JTAG interface simplifies debugging
- Industrial operating temp: -40°C to +85°C



### Description

*The FS471/472 is a video encoder device specifically designed for battery operated handheld device such as Personal Media Players, Smartphones, portable Auto Navigation Systems and other similar devices.*

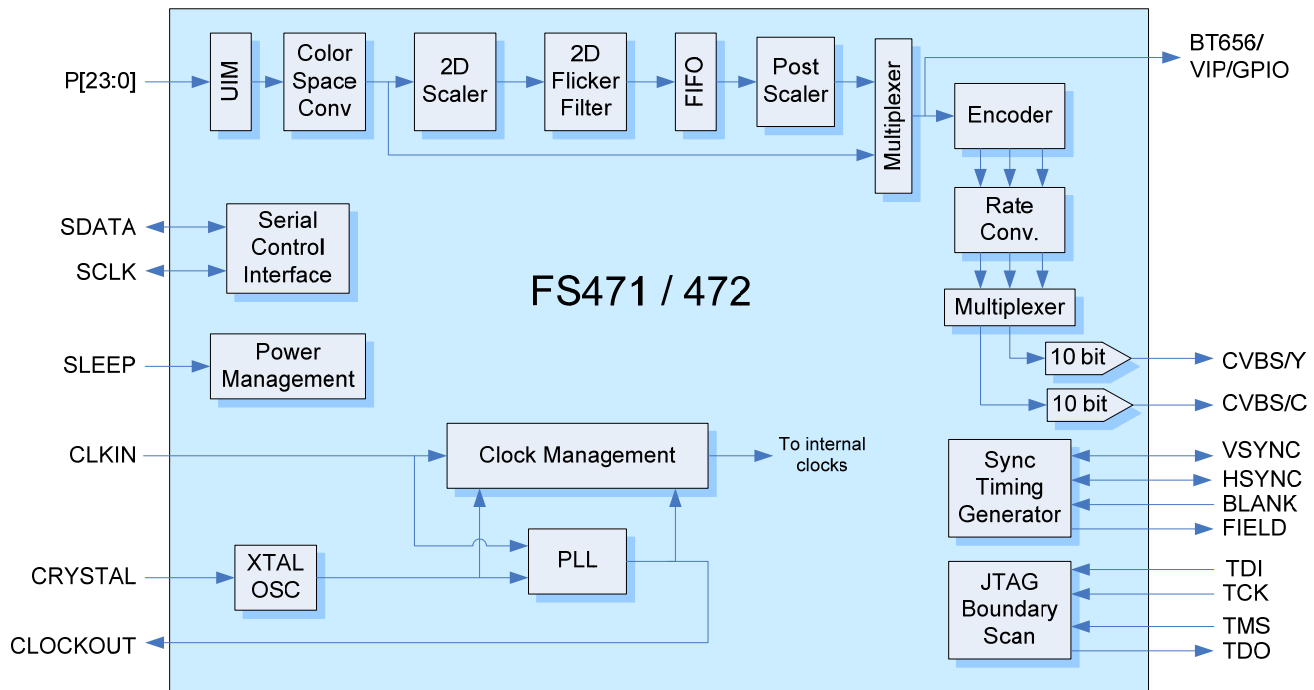
*The FS471/472 maintains the demonstrated quality and benefits of Focus Enhancements' current line of video encoders, provides additional flexibility to system designers and integrates a highly optimized power management engine that enables long battery life without compromising performance.*

*The FS471/472 accepts various data inputs, including RGB and YCrCb, through a programmable digital input interface that supports 24 / 18 / 16 / 15 / 12 / 8 bit pixel data lengths. The digital inputs are converted, scaled, (using patented artifact free scaling and flicker reducing techniques) interlaced, and then encoded into NTSC or PAL analog formats.*

### Applications

**Personal media players — Smart Phones — Handheld Gaming Platforms  
Portable Navigation Systems — Portable DVD players — Cameras and Camcorders  
Others**

## Functional Block Diagram



## Features

### Image Quality

#### *Advanced 2D Flicker Filter*

Focus Enhancements' Patented filtering technique reduces flicker to maintain text readability. This filter technology is significantly more effective than typical three-line-average flicker filters.

#### *Advanced 2D Scaler*

Patented, flexible scaler enables graphics images to be independently upscaled and downscaled in the horizontal and vertical directions to precisely fit TV screen without creating artifacts or blank borders. Scaling flexibility allows many image sizes to be accurately scaled to video dimensions. Extended programmability allows custom-tailoring for a wide range of display devices.

### Pixel clock synchronization

The FS471/472 operates in both master and slave mode.

In master mode, a 2.5MHz-85MHz clock is generated from the 3MHz-30MHz input crystal and supplied to the host graphic controller.

In slave mode, the FS471/472 can accept an input pixel clock between 2.5 and 85MHz.

The FS471/472 can accommodate a wide variety of pixel and line timing within a frame-synchronous system. This flexibility allows the Graphics Controller to provide to the FS471/472 the same clock used for most LCDs. Besides minimizing overall system design effort, this allows both LCD and TV-OUT to remain simultaneously active for many LCD's.

## Interfaces

### *Serial Control Interface*

The FS471/472 hosts a serial input/output bus (SIO) which is compatible with both I<sup>2</sup>C\* and SMBus specifications.

Through this interface the host graphics controller can configure and query the control registers of the FS471/472 anytime during its active and stand-by states.

### Digital Input Interface

The FS471/472 provides a programmable 24-bit/18-bit/16-bit/15-bit/12-bit/8-bit input interface.

Various RGB and YCrCb data formats and resolutions are supported, including the following most commonly used examples:

|          |          |          |
|----------|----------|----------|
| 220x176  | 256x192  | 320x240  |
| 440x234  | 480x234  | 480x272  |
| 640x480  | 720x480  | 720x576  |
| 800x480  | 800x600  | 1024x720 |
| 1024x768 | 1152x864 | 1280x720 |
|          | 1366x768 |          |

### Advanced TV support

The FS471/472 supports both singly and doubly terminated configurations.

It also features proprietary enhancements that enable the system designer to support DC-coupled and AC-coupled TV inputs alike with no degradation in video quality.

### Digital Output Interface (BT.656/VIP/GPIO)

The FS471/472 provides a 4:2:2 YCrCb 8-bit Digital Parallel Interface, conformant to both ITU-R BT.656 and VESA VIP specifications.

Alternatively this interface can also be used as an 8 bit General Purpose Input / Output port (GPIO).

### Analog Output Interface

The two 10 bit DACs can be configured to output S-Video or Composite Video.

When S-Video is selected, both Analog luminance (Y) and chrominance (C) information is available on the Y and C outputs for interfacing to S-video equipment.

When composite is selected the composite analog video signal can be output simultaneously onto one or two analog outputs.

The FS472 includes Macrovision 7.1.L1 copy protection

Supports multiple output formats, including the following:

|             |           |
|-------------|-----------|
| NTSC        | NTSC-EIAJ |
| PAL-B/G/H/I | PAL-M     |
| PAL-N       | PAL-60    |

### Power management

The FS471/472 contains advanced power management configuration options that makes it the ideal solution for battery-powered handheld devices.

### Load Sensing

The FS471/472 can check for the presence of a load and write the load status to a register when commanded by the application processor. This enables the processor to periodically monitor load status and place the FS471/472 in an optimal power savings mode without the need for additional circuitry.

### Active Modes

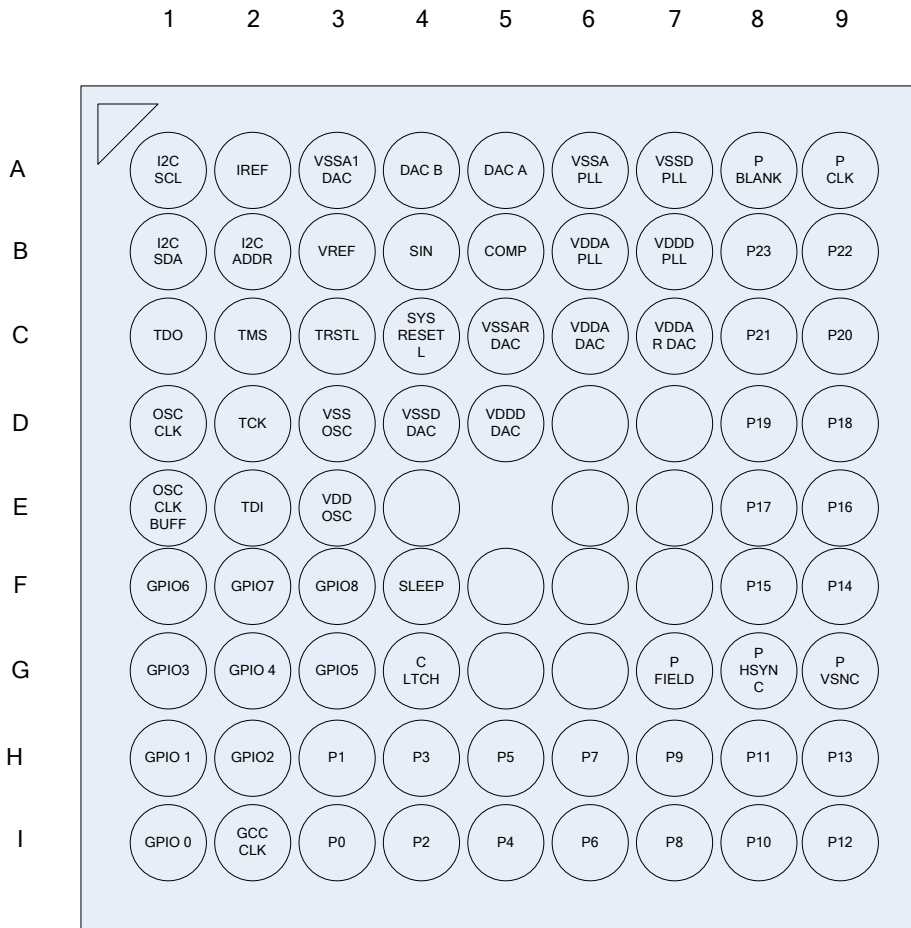
|             | Typical Power Consumption |                    |
|-------------|---------------------------|--------------------|
|             | Single termination        | Double termination |
| S-Video     | 200mW                     | 300mW              |
| Composite   | 140mW                     | 180mW              |
| Digital Out | -                         | 100mW              |

### Power Saving Modes

|            | Average Power Consumption                       |
|------------|---|
| Stand-By   | 100mW   |
| Sleep      | 20uA  |
| Deep Sleep | 500nA<br><i>(requires additional circuitry)</i> |

### Development and Testing

Four input/output pins are dedicated to JTAG/IEEE 1149.1 to support real-time debugging, monitoring and boundary-scan tests.



**80 Pin BGA (Top View)**

**Ball Assignments**

| Ball name   | Ball #   | Type   | Description  |
|-------------|--|--------|--|
| P23-0       | I3,H3,I4,H4,I5,H5,I6,H6,<br>I7,H7,I8,H8,I9,H9,F9,F8,E9,<br>E8,D9,D8,C9,C8,B9B8 | Input  | Digital pixel data input port.<br>ITU-R BT.656/601 data input port |
| P_CLK       | A9   | Input  | Pixel Clock Input  |
| P_HSYNC     | G8   | In/Out | Digital HSYNC VGA  |
| P_VSYNC     | G9   | In/Out | Digital VSYNC.   |
| P_FIELD     | G7   | Output | Digital HSYNC  |
| P_BLANK     | A8   | Input  | Digital Blank  |
| OSC_CLK     | D1   | Input  | TV reference clock (crystal) input                                 |
| OSC_CLK_BUF | E1   | Output | Buffered TV reference clock  |

## Ball Assignments—continued

| Ball name  | Ball #                         | Type          | Description   |
|------------|--------------------------------|---------------|---|
| GCC_CLK    | J2                             | Output        | Pixel Clock Output  |
| SYS_RESETL | C4                             | Input         | System Reset  |
| GPIO0-8    | J1,H1,H2,G1,<br>G2,G3,F1,F2,F3 | In/Out        | General Purpose Input / Output.<br>GPIO0-7 can also be configured as<br>BT.656 outputs. |
| CLTCH      | G4                             | Input         | Retention I/O Enable  |
| SLEEP      | F4                             | Input         | Sleep input   |
| TCK        | D2                             | Input         | Test Clock  |
| TMS        | C2                             | Input         | Test Mode Select  |
| TDI        | E2                             | Input         | Test Data Input   |
| TDO        | C1                             | Output        | Test Data Output  |
| TRSTL      | C3                             | Input         | Test Reset  |
| I2C_SCL    | A1                             | Input         | Serial Data Clock   |
| I2C_SDA    | B1                             | In/Out        | Serial Data   |
| I2C_ADDR   | B2                             | Input         | Serial data address select  |
| SIN        | B4                             | Analog Input  | Compensation  |
| IREF       | A2                             | Analog Input  | External Resistor sets DAC current  |
| DAC_A      | A5                             | Analog Output | Video Output  |
| DAC_B      | A4                             | Analog Output | Video Output  |
| COMP       | B5                             | Analog Output | Compensation  |
| VDDA_PLL   | B6                             | Power         | Phase Locked Loop Analog Power  |
| VDDD_PLL   | B7                             | Power         | Phase Locked Loop Digital Power   |
| VSSA_PLL   | A6                             | Ground        | Phase Locked Loop Analog Ground   |
| VSSD_PLL   | A7                             | Ground        | Phase Locked Loop Digital Ground  |
| VDD_OSC    | E3                             | Power         | TV Crystal Oscillator Power   |
| VSS_OSC    | D3                             | Ground        | TV Crystal Oscillator Ground  |
| VDDA_DAC   | C6                             | Power         | DAC Analog Power  |
| VDDD_DAC   | D5                             | Power         | DAC Digital Power   |
| VSSA1_DAC  | A3                             | Ground        | DAC Analog Ground   |
| VSSD_DAC   | D4                             | Ground        | DAC Digital Ground  |
| VDDAR_DAC  | C7                             | Power         | DAC Analog Power  |
| VSSAR_DAC  | C5                             | Ground        | DAC Analog Ground   |
| VREF       | B3                             | Power         | DAC Reference Voltage   |

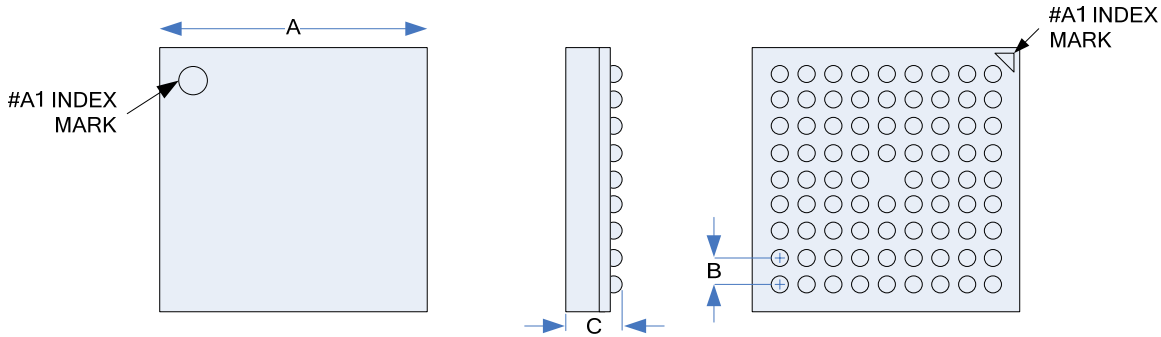
## Electrical

|           | Description                     | Min.    | Typical        | Max.   |
|-----------|---------------------------------|---------|----------------|--------|
| VDDA_PLL  | Phase-Locked Loop Analog Power  | +2.85 V | +3.3 V         | +3.6V  |
| VDDD_PLL  | Phase Locked Loop Digital Power | +1.35V  | +1.5V          | +1.65V |
| VDD_OSC   | TV Crystal Oscillator Power     | +2.85 V | +3.3 V         | +3.6V  |
| VDDA_DAC  | DAC Analog Power                | +2.85 V | +3.3 V         | +3.6V  |
| VDDD_DAC  | DAC Digital Power               | +1.35V  | +1.5V          | +1.65V |
| VDDAR_DAC | DAC Analog Power                | +2.85 V | +3.3 V         | +3.6V  |
| VREF      | DAC Reference Voltage           |         | .1uF Capacitor |        |
| VDD_CORE  | Digital Core Power              | +1.35V  | +1.5V          | +1.65V |
| VDD_IO    | Digital I/O Voltage             | +1.65 V | -              | +3.3 V |

## Temperature range

Designed and tested to support an industrial temperature range of -40°C to +85°C.

## Mechanical



The FS471/472 is offered in the following RoHS compliant package:

| Package | Pins | Size (A) | Pitch (B) | Profile (C) |
|---------|------|----------|-----------|-------------|
| BGA     | 80   | 5mm      | 0.5mm     | 1.0mm       |

\*Note:  $I^2C$  is a registered trademark of Philips Corporation. The FS471/472 serial input/output bus is similar but not identical to the Philips  $I^2C$  bus.



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